

# Five dollar 300 baud modem

Professor Yoshiyasu Takefuji of the Center for Machine Intelligence, University of South Carolina, describes a 300 baud low cost full duplex modem.

The MODEM or MODulator/DEModulator serves as the connecting link for digital equipment to communicate over telephone lines. The modem encodes (modulates) incoming data into signals suited for transmission over telephone lines, and the modem also decodes (demodulates) signals received from the telephone line. A modem is required at each end of the phone line to encode and to decode the data sent between digital devices. The modem initiating the conversation is called the originate modem and the receive modem the answer. Modems with the ability to communicate in both directions simultaneously are called full duplex, half duplex is communication in one direction at a time, and simplex is one way communication. Modem speeds of transmitting and receiving are specified in BPS (Bit per second). This term describes the number of binary data bits that can be transmitted per second. For low speed modems, baud rate is interchangeable and used in place of BPS. Most modems are generally classified according to which standard, Bell (US) or CCITT (European), they conform to. There are two popular kinds of modulation techniques, FSK and PSK. FSK, or Frequency Shift Keying, encodes binary data into the two discrete frequencies. With the FSK scheme the higher frequency is known as the Mark frequency and the lower is the Space (figure 1).

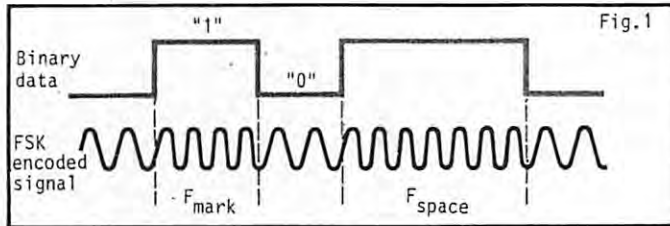


Figure 1: FSK encoding

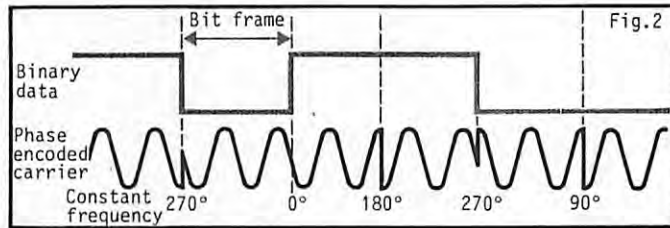


Figure 2: PSK encoding

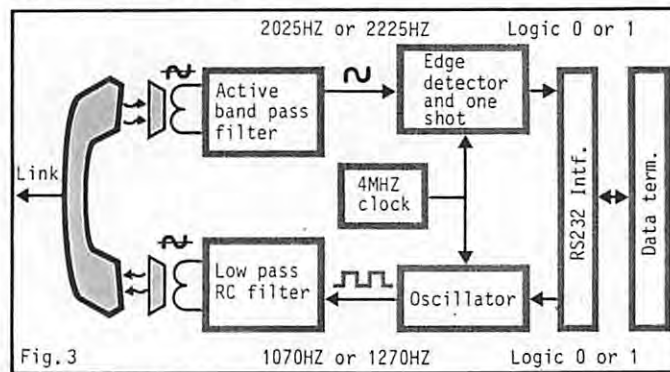


Figure 3: Block diagram of the modem

In PSK (Phase Shift Keying) a constant carrier frequency is used with the relative phase of it indicating the value of the binary data bit. Because the relative, not absolute, phase of the carrier is important, most PSK schemes are DPSK or Dibit PSK. DPSK measures the phase of the carrier in two successive bit frames in order to determine the phase change. PSK encoding in the Bell 212A standard is shown in figure 2.

This project is to construct a 300 baud full duplex originate modem. The 300 baud originate signal is sent at 2025/2225Hz and an answer signal is sent at 1070/

1270Hz. The aim of this project is to provide an exercise in the application of digital techniques to the problem of interfacing a computer terminal to a telephone link of a computer network. The type of interface chosen is an acoustically coupled modem.

The modem is to take serial data from the RS232c port of a computer terminal and convert the logic levels to a frequency (logic 1=1270Hz, logic 0=1070Hz), and acoustically couple this frequency shift logic to a telephone link to establish communication with a computer network. Information returning from the network is transmitted along the telephone link as a frequency shift logic (logic 1=2225Hz, logic 0=2025Hz) and then acoustically coupled to the modem where the frequency shift is converted to logic levels and transferred to the RS232c port of a computer terminal. A block diagram of modem is shown in figure 3. The detailed modem circuit is described in figure 4.

## Receive section

FSK data from the telephone link is acoustically coupled to the modem from a telephone hand set to an 8 ohm 2 inch speaker, producing a low level electrical waveform containing both signal information and coupled noise. This low level waveform is amplified to a more workable level by an operational amplifier (U1-a), resistors R1 and R2, and capacitor C1. (figure 5)

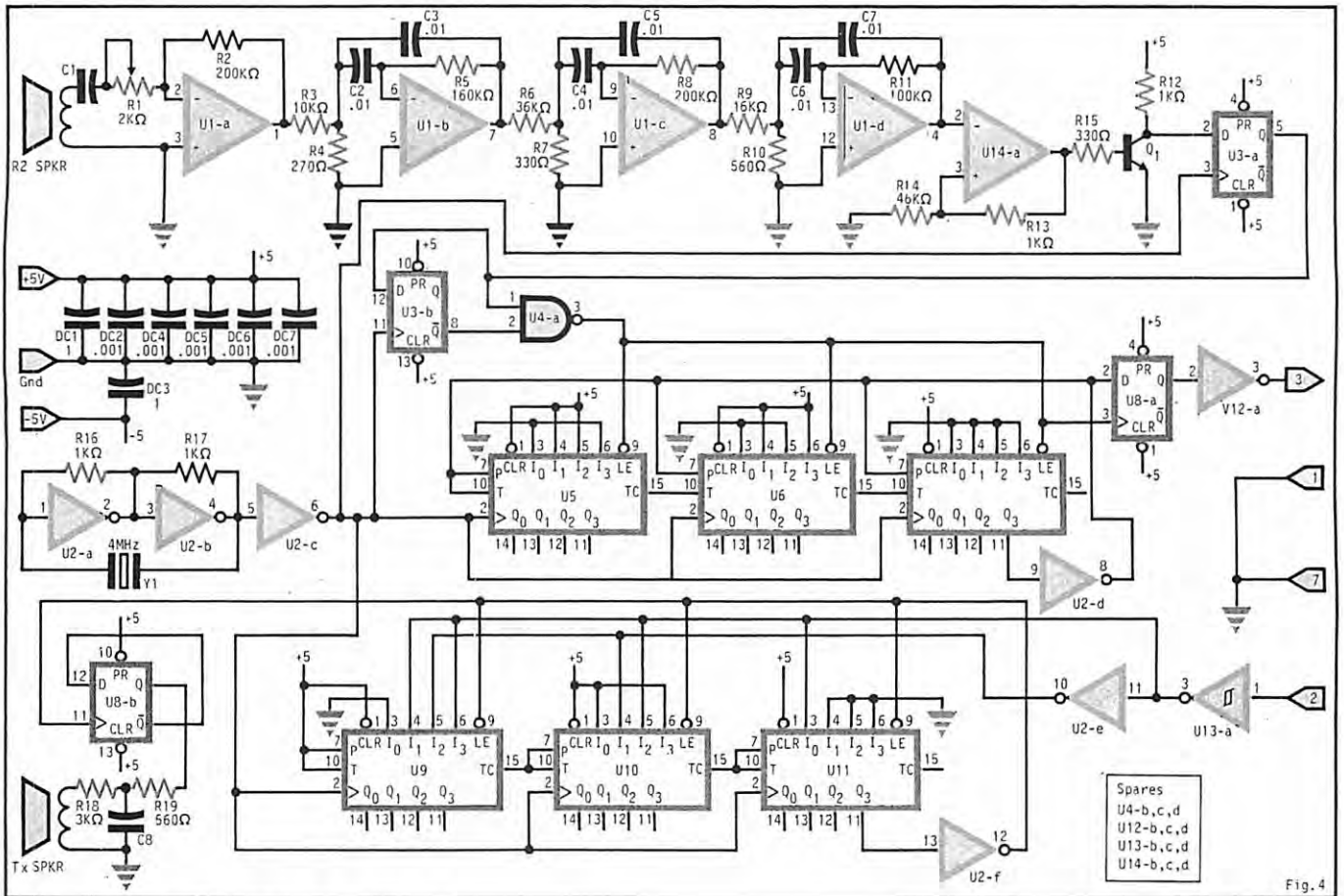


Figure 4: Circuit diagram of the modem

Capacitor C1 is large enough so that at the lowest desired frequency level received its impedance becomes small enough to be ignored in gain calculations. Therefore amplifier gain becomes:

$$A = R2/R1$$

with R1 adjustable to compensate for varying speaker characteristics. A two- or three-stage active filter is used to selectively amplify the desired frequencies and discriminate against all undesired frequencies. The first stage of the filter selectively amplifies a band of frequencies including the frequency representing a logic 1 (2225Hz). The second stage selectively amplifies a band of frequencies including the frequency representing a logic 0 (2025Hz). The third stage of the filter is a band pass filter designed to pass both the upper and lower operating frequencies representing logic 1 and 0. The characteristics of each stage of the active filter can be found by figure 6.

The signal exiting the active filter still has frequencies outside those acceptable by the Bell 103 standard but at a much lower ampli-

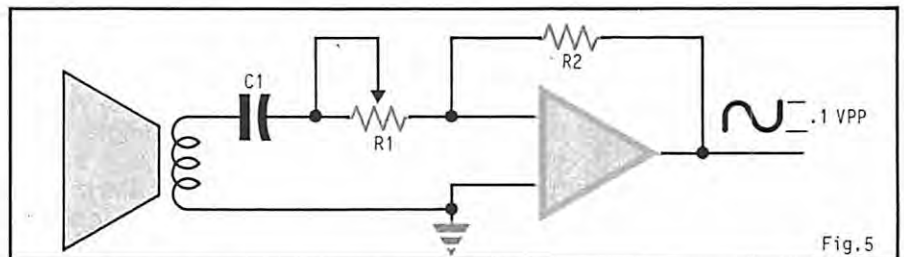


Figure 5: First stage amplification

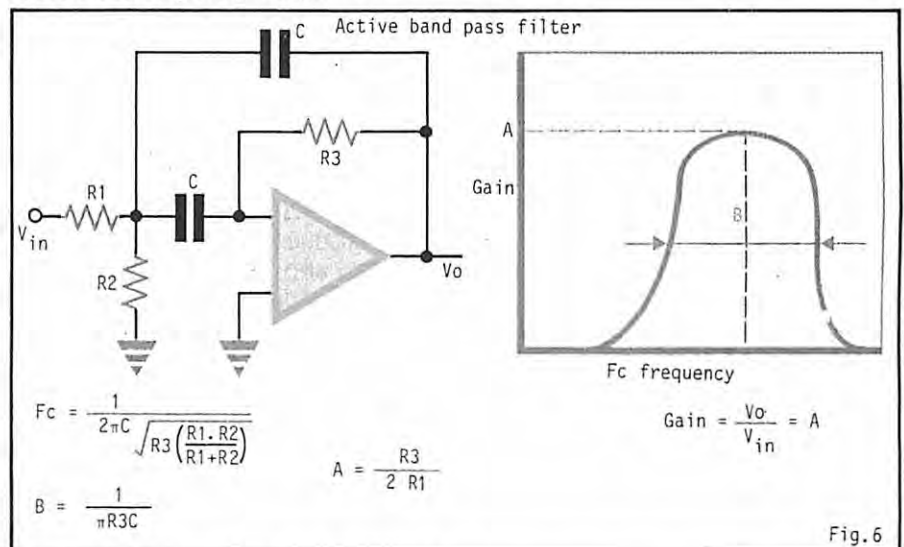


Figure 6: Characteristics of active bandpass filter

tude. A very high gain hysteresis stage is added to provide a square wave type signal at the frequency of the received data signal passed by the active filter. The unwanted frequencies should be less than +0.1V peak-to-peak and can be eliminated by a hysteresis of +0.1V peak-to-peak shown in figure 7. This square wave signal is converted to a TTL level signal by transistor Q1 and resistor R13, R15 by clipping the negative part of the wave. There should be an approximate TTL square waveform with frequencies of 2225Hz or 2025Hz (plus or minus a small frequency deviation), which can be converted to a TTL level by use of a positive edge extractor and a one-shot circuit. The positive edge extractor generates the edge pulse, which is used to load a binary 166 into the one-shot circuit composed of synchronous counters. The one-shot circuit will generate an output after 1882 counts of the 4MHz clock, which is inverted and stops the counter from counting until the next positive edge load pulse starts the sequence over again. This time period is approximately 470 microseconds and corresponds to the period of the frequency midway between 2025Hz and 2225Hz. This provides a reference time period, if the period of received signal is  $1/2225$  seconds then this is less than the time required for the one-shot to time out, therefore the one-shot will be reset and the output will remain high corresponding to a logic 1. If the period of the signal received is  $1/2025$  second then the one-shot will time out after each load pulse, producing a low at its output until the next load pulse. The D-Flip-Flop is used to clock the one-shot output to the RS232c interface on the next load pulse from the positive edge extractor. This causes a logic 0 to remain continuously low as long as 2025Hz is being received and the one-shot is allowed to time out.

**Transmit section**

RS232c logic levels are received by an MC1489 receiver, and converted to TTL logic levels. An oscillator composed of synchronous counters converts the logic levels to a stream of negative pulses at twice the frequency of that required

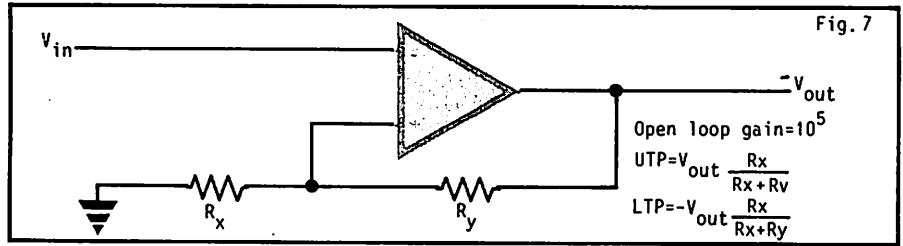


Figure 7: High-gain hysteresis stage to provide square-wave signal

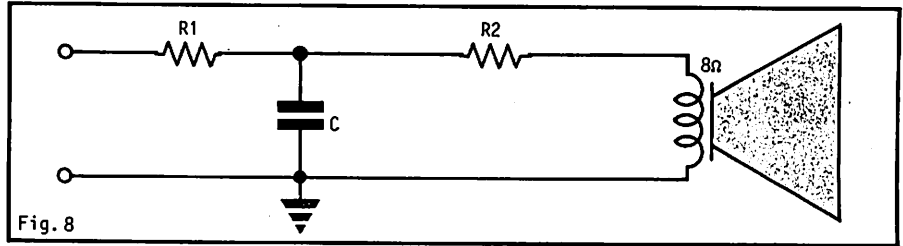


Figure 8: Low pass RC filter and voltage divider to provide output

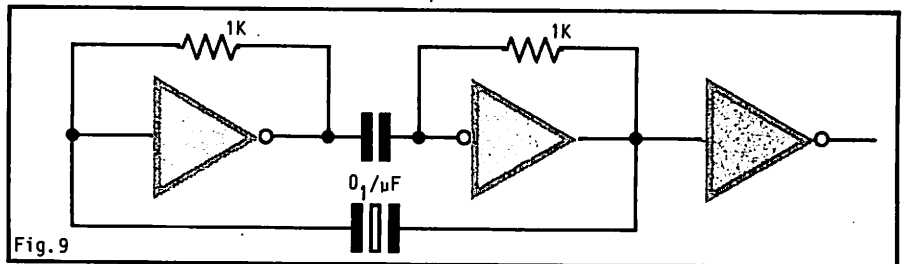


Figure 9: System clock

for a logic one or zero as per the Bell 103 standard for data transmitted by a modem in the originate mode. A logic one from the RS232c receiver is applied to the appropriate data inputs of the synchronous counters of the transmit oscillators to allow loading a binary 474 into the counters. At a counter of 1575 cycles of the 4MHz clock the 2048 output of the counters produces an output that is inverted and used to reload the counters and produce a low pulse. When the RS232c receiver's output is a logic 0, its output is inverted and applied to the appropriate data input of the synchronous counter to load a binary 180. At a count of 1869 clock cycles of the 4MHz clock the 2048 output of the counters produces an output that is inverted and used to reload the counters and produce a low pulse. The stream of pulses produced by the counters are approximately 0.25 micro seconds long once every load cycle of the oscillator and at twice the desired frequency. This stream of pulses is fed to the clock input of a D-Flip-Flop used as a divide-by-2 counter producing a symmetrical square wave at the

frequency required (1070Hz=logic 0, 1270Hz=logic 1). This frequency is at TTL levels and a square wave still not suitable to be transmitted over the telephone. A low pass RC filter and voltage divider, (see figure 8) is used to convert the square wave to an approximate sine wave of an appropriate level to acoustically couple to the telephone link.

**System clock**

The system clock in figure 9 is a crystal controlled oscillator composed of inverters, resistors, and a crystal. The oscillator generates a square wave at 4MHz and is buffered by inverter to prevent loading of the clock and drive sufficient to supply all of the system clock inputs.

It is fairly easy to implement the 300 baud modem if it is known how to manage the grounding and connections. More applications of edge extractors and one-shot circuits using synchronous counters are referred to in the Logic design manual. □

**References**

1. Yoshiyasu Takefuji, 'Logic design manual', University of South Carolina, Jan. 1986.